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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,120	06/23/2003	Hadj L. Mokeddem	P16169	1101

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EXAMINER	
CHANG, JOSEPH	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,120	MOKEDDEM, HADJ L.	
	Examiner	Art Unit	
	Joseph Chang	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *04 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12 and 25-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12 and 25-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The text of those sections of Title 35 U.S.C. Code not included in this action can be found in a prior Office action.

Claims 1-5 and 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Girard et al. US Pat. No. 5,760,640.

Regarding Claim 1, Girard et al. disclose in Figure 3 a charge pump (bi-direction current sources - charging and pumping currents) comprising: a first PMOS transistor (T8); a first NMOS transistor (T9) coupled to the first PMOS transistor (T8) via a first common drain node (**15**); a second PMOS transistor (T6); a second NMOS transistor (T7) coupled to the second PMOS transistor (T6) via a second common drain node (**14**); a first current source (T2) coupled to respective source terminals (16) of the first and second PMOS transistors (T6,T8); a second current source (T5) coupled to respective source terminals (17) of the first and second NMOS transistors (T7, T9); a first operational amplifier (OP1)having a first input ("+", not shown) coupled to the first common drain node (14) and a second input ("-", not shown) coupled to the second common drain node (15) and an **output (15) directly coupled to the second common drain node** (a feedback line connecting from the output of the OP1 to the inverting side of the inputs (not shown) is inherently present because the OP1 is to maintain its gain equal to one i.e. a voltage follower)(Col.1, lines 55-60); a reference circuit (T1,T3,T10,20,T11,T12); and a second operational amplifier (OP2) having a first input

("-") **directly** coupled to the first common drain node (**15**) and a second input ("+") coupled to the reference circuit (20).

Regarding Claim 2, a capacitor coupled to the first common drain node (15, output of the charge pump) is inherently and necessary present because the capacitor at the output of charge pump is to charge or pump the currents from the current sources.

Regarding Claim 3, Figure 3 shows the reference circuit includes: a third PMOS transistor (T10); a third NMOS transistor (T11) coupled to the third PMOS transistor (T10) via a third common drain node (20); a third current source (T3) coupled to a source terminal (source of T10) of the third PMOS transistor (T10); and a fourth current source (T12) coupled to a source terminal (source of T11) of the third NMOS transistor (T11); wherein the second input ("+") of the second operational amplifier (OP2) is coupled to the third common drain node (20).

Regarding Claim 4, Figure 3 shows the first current source (T2) is a PMOS current Source.

Regarding Claim 5, Figure 3 shows the second current source (T5) is an NMOS current source.

Regarding Claim 25, Girard et al. discloses in figure 3, a charge pump (bi-direction current sources - charging and pumping currents) comprising: an output terminal (**15, see also col.4, lines 60-62**); a first element (T8) to control charging of the output terminal (**15**); a second element (T9) to control discharging of the output terminal (**15**) and including a common node (15, same as the output terminal) with the first

element (T8); a reference circuit (T1, T3, T10, 20,T11, T12); and an operational amplifier (OP2) including a first input ("-") **directly** coupled to the **output terminal** (15) and a second input ("+") coupled to the reference circuit (20).

Regarding Claims 26 and 27, Figure 3 shows the first element (T8) comprises a PMOS transistor and the second element (T9) comprises an NMOS transistor.

Regarding Claim 28, Figure 3 shows the reference circuit includes: a first transistive element (T10); a second transistive element (T11) coupled to the first transistive element (T10); a first current source (T3) coupled to the first transistive element (T10); and a second current source (T12) coupled to the second transistive element (T11).

Regarding Claim 29, Figure 3 shows the first transistive element (T10) comprises a PMOS transistor and the second transistive element (T11) comprises an NMOS transistor.

Regarding Claim 30, Figure 3 shows the first and second transistive elements (T10, T11) include a common drain node (20); and the second input ("+") of the operational amplifier (OP2) is coupled to the common drain node (20).

Regarding Claims 31, Figure 3 shows a second output terminal (**14**), and a second operational amplifier (OP1) including a first input coupled to the common mode (15) and a second input coupled to the second output terminal (14) ("a first input coupled to the common mode (15)" is not shown in the OP1, in other words a feedback line connecting from the output of the OP1 to the inverting side of the input of OP1 is

inherently present because the OP1 is to maintain its gain equal to one as a voltage follower; Col.1, lines 55-60).

Claims 8-12 and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz et al., US Pat. No. 5,950,115 in view of Girard et al. US Pat. No. 5,760,640.

Regarding Claims 8-12 and 32-38, Momtaz et al. discloses in Figures 1-3 an apparatus (transceiver) a communication port (Dout or Din) and a serializer/deserializer (32, 38) coupled to the communication port (Dout or Din) serializer/deserializer (32, 38) including a phase locked loop (20, 28) except for a specific charge pump as discussed above in claim rejections 1-5 and 25-31 as being anticipated by Girard et al.

Girard et al. further teaches that his chare pump provides a highly symmetrical bi-directional current sources so that it eliminates unwanted potential differences exist in a conventional charge pump, and also it provides excellent impedance matching at all paths between supply voltages.

Accordingly, it would have been obvious to one of ordinary skill in the art to at the time of the invention to substitute a charge pump, as taught by Girard et al, for the charge pump of Momtaz et al. because such modification would have provided a highly symmetrical bi-directional current sources so that it eliminates unwanted potential differences exist in a conventional charge pump as taught by Girard et al..

Regarding Claim 8, Figure 3 shows a second operational amplifier (OP2) having a first input ("-") directly coupled to the first common drain node (15), a second input

("+") coupled to the reference circuit (20), and an output (21) coupled to a gate terminal of the first current source (T2, via T5 and 12). It is noted that the recitation "coupled to" is a broad term that any points in a given circuitry are considered "coupled to" unless there is a modifier such as "directly" coupled to.

Claim 1-5, 7, 25-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desortiaux US Pub. No. 2003/0122626 in view of Momtaz US Pat. No. 5945855.

Regarding Claims 1, 25, 31, Desortiaux disclose in Figure 1 a charge pump comprising: a first PMOS transistor (M15); a first NMOS transistor (M16) coupled to the first PMOS transistor (M15) via a first common drain node (**7**); a second PMOS transistor (M13); a second NMOS transistor (M14) coupled to the second PMOS transistor (M13) via a second common drain node (**6**); a first current source (M1) coupled to respective source terminals (4) of the first and second PMOS transistors (M15, M13); a second current source (M3) coupled to respective source terminals (5) of the first and second NMOS transistors (M16,M14); a reference circuit (1, M2,M11,2,M8,M10,M9,M7,3,M12,M4); and a second operational amplifier (AOP1) having a first input ("-") **directly** coupled to the first common drain node (**7**) and a second input ("+") coupled to the reference circuit (2).

However, Desortiaux does not show "a first operational amplifier having a first input coupled to the first common drain node and a second input coupled to the second common drain node and an output directly coupled to the second common drain node".

As would have been well known in the art, such a configuration of operational amplifier connections is used at the common drain nodes to maintain the same potential for symmetry requirements on the signal paths of the pump-up and pump-down. Momtaz, for example, shows in Figure 4 the operational amplifier having such connections.

Accordingly, it would have been obvious to one of ordinary skill in the art to at the time of the invention to add circuitry of operational amplifier as shown in Momtaz at the two common drain nodes of the Desortiaux because such modification would have provided the benefit of maintaining the same potential for symmetry requirements on the signal paths of the pump-up and pump-down.

Regarding Claims 7, Figure 1 of Desortiaux shows an output of the second operational amplifier (AOP1) is directly coupled to a gate terminal of the first current source (M1).

Regarding Claims 2, a capacitor coupled to the first common drain node (7, output of the charge pump) is inherently and necessary present because the capacitor at the output of charge pump is to charge or pump the currents from the current sources.

Regarding Claims 3, 28-30, Figure 1 of Desortiaux shows the reference circuit includes: a third PMOS transistor (M11); a third NMOS transistor (M8) coupled to the third PMOS transistor (M11) via a third common drain node (2); a third current source (M2) coupled to a source terminal of the third PMOS transistor (T11); and a fourth current source (M4) coupled to a source terminal of the third NMOS transistor (M8);

wherein the second input ("+") of the second operational amplifier (AOP1) is coupled to the third common drain node (20). It is noted that the recitation "coupled to" is a broad term that any points in a given circuitry are considered "coupled to" unless there is a modifier such as "directly" coupled to.

Regarding Claims 4, Figure 1 of Desortiaux shows the first current source (M1) is a PMOS current Source.

Regarding Claim 5, Figure 1 of Desortiaux shows the second current source (M3) is an NMOS current source.

Regarding Claims 26-27, as discussed above in claims 4-5, Figure 1 of Desortiaux shows the first and second PMOS and NMOS elements.

Claims 8-12 and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momtaz et al., US Pat. No. 5,950,115 as applied to claims 1-5, 7, 25-31 above (as being unpatentable over Desortiaux US Pub. No. 2003/0122626 in view of Momtaz US Pat. No. 5945855).

Regarding Claims 8-12 and 32-38, Momtaz et al. discloses in Figures 1-3 an apparatus (transceiver) a communication port (Dout or Din) and a serializer/deserializer (32, 38) coupled to the communication port (Dout or Din) serializer/deserializer (32, 38) including a phase locked loop (20, 28) except for a specific charge pump as discussed above in claim rejections 1-5, 7, and 25-31 as being unpatentable over Desortiaux US Pub. No. 2003/0122626 in view of Momtaz US Pat. No. 5945855.

Desortiaux in view of Momtaz US Pat. No. 5945855 teaches that his chare pump provides a highly symmetrical bi-directional current sources so that it eliminates unwanted potential differences exist in a conventional charge pump, and also it provides a wide output voltage range to maximize the adjustment range of a VCO in a PLL circuit.

Accordingly, it would have been obvious to one of ordinary skill in the art to at the time of the invention to substitute a charge pump, as taught by Desortiaux US Pub. No. 2003/0122626 in view of Momtaz US Pat. No. 5945855, for the charge pump of Momtaz et al. US Pat. No. 5,950,115 because such modification would have provided a highly symmetrical bi-directional current sources so that it eliminates unwanted potential differences exist in a conventional charge pump and also provided a wide output voltage range to maximize the adjustment range of a VCO in a PLL circuit as taught by Desortiaux in view of Momtaz US Pat. No. 5945855.

Response to Arguments

Applicant's arguments with respect to claims 1-5, 7-12, 25-38 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Chang whose telephone number is 571 272-1759. The examiner can normally be reached on Mon-Fri 0700-1730.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JC

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